What is claimed is:

1. A semiconductor device comprising:

a substrate of a first conductivity type,

multiple output pad terminals arranged linearly on a surface of the substrate,

high-voltage drive transistor and electrostatic protection transistor pairs connected in series between the output pad terminals and a power supply line, and

a drive control circuit for controlling gates of the high-voltage drive transistors.

2. A semiconductor device according to claim 1, wherein the high-voltage drive transistors and the electrostatic protection transistors are MOSFET transistors and a channel length of the electrostatic protection transistors and is shorter than a channel length of the high-voltage drive transistors.

3. A semiconductor device according to claim 1, wherein a drain withstand voltage of the electrostatic protection transistors is lower than a drain withstand voltage of the high-voltage drive transistors.

4. A semiconductor device comprising:

an electrostatic protection transistor having a drain region electrically connected with an output pad terminal, a source region electrically connected with a power source line, and a gate electrically connected with the power source line,

the drain region being constituted of a low-concentration drain region of a second conductivity type formed on a surface of a semiconductor region of a first conductivity type and a high-concentration drain region formed on a surface within the low-concentration drain region, and

the gate being formed on a field insulating film formed on the semiconductor region between the source region and the low-concentration drain region.

5. A semiconductor device according to claim 4, wherein a field doped region of a first conductivity type having a higher concentration than the semiconductor region is formed on the surface of the semiconductor region between the source region and the low-concentration drain region.

6. A semiconductor device according to claim 4, wherein the source region includes a high-concentration source region and a low-concentration source region symmetrical with the drain regions.

7. A semiconductor device according to claim 4, further comprising a MOSFET transistor of the second conductivity type formed on the surface of the semiconductor region, a well of the second conductivity type formed on the surface of the semiconductor region and a MOSFET transistor of the first conductivity type formed on the surface of the well, the low-concentration drain r gion and the well having the same impurity distribution.

8. A semiconductor device comprising:

a source region of a second conductivity type formed on a surface of a semiconductor substrate of a first conductivity type,

a first drain region of the second conductivity type formed on the surface of the semiconductor substrate to be separated from the source region by a channel-forming region,

a second drain region of the second conductivity type formed on the surface of the semiconductor substrate in contact with the first drain region,

a gate formed on the channel-forming region via a gate insulating film, and

a punch-through prevention region of the second conductivity type formed on the surface of the semiconductor substrate where the channel-forming region and the first drain region are in contact,

the first drain region being formed to a deeper diffusion depth and lower surface concentration than the second drain region and the punch-through prevention region being formed to a deeper diffusion depth than the second drain region.

9. A semiconductor device according to claim 8, further comprising a field insulating film of greater thickness than the gate insulating film formed between an end portion of the gate and the first drain region.

10. A semiconductor device according to claim 8, wherein the punch-through prevention region and the

second drain r gion are formed in self-alignment with the field insulating film.

11. A semiconductor device according to claim 8, further comprising a second source region of the same impurity distribution as the first drain region formed between the source region and the channel-forming region.

12. A semiconductor device comprising:

a first diffused region of a first conductivity type formed over a whole surface of a semiconductor substrate of a first conductivity type to have a higher concentration than the substrate and

second and third diffused regions of a second conductivity type formed on the surface of the substrate to a depth of not less than 1.0 μm at locations separated by 1.0 - 5.0 μm to have a higher concentration than the first diffused region.

13. A semiconductor device according to claim 12, further comprising field-effect transistors respectively utilizing first and second insulating films and respectively formed on surfaces of the second and third diffused regions.

14. A semiconductor device according to claim 13, wherein the first diffused region is formed to a depth between that of source and drain regions of the field-effect transistors utilizing the first and second insulating films and that of the second and third diffused regions.

15. A semiconductor device comprising:

a source region of a second conductivity type formed on a surfac of a semiconductor region of a first conductivity type,

a first drain region of the second conductivity type formed on the surface of the semiconductor region to be separated from the source region by a channel-forming region,

a second drain region of the second conductivity type formed on the surface of the semiconductor region in contact with the first drain region,

a gate formed on the channel-forming region via a gate insulating film and the first drain region via a field insulating film, and

an impurity region containing more first conductivity type impurity element than the semiconductor region formed on a surface of the first drain region.

16. A semiconductor device comprising:

a low-drain-withstand-voltage MOSFET transistor of a second conductivity type formed on a surface of a semiconductor region of a first conductivity type and

a high-drain-withstand-voltage MOSFET transistor formed on the surface of the semiconductor region to be separated from the low-drain-withstand-voltage MOSFET transistor by an isolation region,

the isolation region including a field doped region of a first conductivity type formed on the surface of the semiconductor region to have a higher concentration

than the semiconductor region and a field insulating film formed on the field doped region, and

a drain region of the high-drain-withstand-voltage MOSFET consisting of an impurity region of the second conductivity type including the field doped region and having a higher concentration than the field doped region.

17. A method of fabricating a semiconductor device including a low-drain-withstand-voltage MOSFET transistor of a second conductivity type formed on a surface of a semiconductor region of a first conductivity type and a high-drain-withstand-voltage MOSFET transistor formed on the surface of the semiconductor region to be separated from the low-drain-withstand-voltage MOSFET transistor by an isolation region, the method comprising the steps of:

forming an oxidation-resistant mask film on a surface of the semiconductor,

selectively etching the oxidation-resistant mask film to remove portions thereof corresponding to the isolation region and a low-concentration drain region of the high-drain-withstand-voltage MOSFET transistor,

implanting portions of the surface of the semiconductor region corresponding to the isolation region and the low-concentration drain region with impurity ions of the first conductivity type using the oxidation-resistant mask film as a mask,

forming a resist film on the surface of the semiconductor region,

removing portions of the resist film corresponding to the low-concentration drain region,

implanting impurity ions of the second conductivity type using the resist film as a mask,

forming a field oxide film by selective oxidation of the surface of the semiconductor region using the oxidation-resistant mask film as a mask, the selective oxidation step forming a field doped region on the surface of the semiconductor region under the field oxide film of the isolation region,

forming the low-concentration drain region and a field oxide film on the low-concentration drain region,

removing the oxidation-resistant mask film and forming a gate insulating film on the surface of the semiconductor region,

patterning gates of the low-drain-withstand-voltage MOSFET transistor and the high-drain-withstand-voltage MOSFET transistor on the gate insulating film, and

forming source and drain regions of the low-drain-withstand-voltage MOSFET transistor and the high-drain-withstand-voltage MOSFET transistor by doping the surface of the semiconductor region with impurity of the second conductivity type using the gates as a mask.

18. A semiconductor device comprising:

first source and drain regions of a first conductivity type formed on a surface of a semiconductor region of a second conductivity type,

second drain and source regions of the first conductivity type formed on the surface of the semiconductor region to be separated from the first source and drain regions by an element isolation region of the second conductivity type,

a field insulating film formed on the element isolation region of the second conductivity type, and

an impurity region containing more first conductivity type impurity element than the semiconductor region formed on a surface of the element isolation region.

19. A semiconductor device comprising a series connection of at least one MOS transistor and a diffused resistance which depletes at a voltage lower than a drain withstand voltage of the MOS transistor.

20. A semiconductor device according to claim 19, comprising a series connection of multiple MOS transistors whose drains are connected together and the diffused resistance.

21. A semiconductor device according to claim 19, wherein at least part of the diffused resistance is of MOS structure.

22. A semiconductor device according to claim 19, wherein the diffused resistance is formed in an isolation region of a MOS integrated circuit.

23. A high-voltage MOSFET semiconductor device comprising:

a source region and a drain region of a second conductivity type formed apart from each other on a surface of a semiconductor region of a first conductivity type,

a gate insulating film formed on a channel-forming region constituted by the surface of the semiconductor region between the source region and the drain region, and

a gate formed on the gate insulating film,

the drain region being constituted of a high-concentration drain region and a low-concentration drain region formed between the channel-forming region and the high-concentration drain region, and

a voltage of the high-concentration drain region during weak inversion or inversion of the channel-forming region being set lower than an applied drain voltage.

24. A high-voltage MOSFET semiconductor device according to claim 23, wherein the channel-forming region between the source region and the low-concentration drain region has a channel length of not more than 2.5 μm and the thickness of the gate insulating film is not more than 200 Å.

25. A high-voltage MOSFET semiconductor device according to claim 23, further c mprising a substrate electrode region of a first conductivity type formed on

the surface of the semiconductor region apart from the source region.

26. A semiconductor integrated circuit comprising:

an HVMISFET (high-drain-withstand-voltage MOSFET) formed on a semiconductor region and having a gate insulating film of a thickness in the range of 100 - 200 Å and

an LVMISFET (low-drain-withstand-voltage MOSFET) of the same conductivity type formed on the same semiconductor region and having the same threshold voltage and gate insulating film as the HVMISFET,

a surface concentration of the semiconductor region directly under the gate insulating film being partially increased to make the threshold voltage not less than 0.7 V and

drain regions and source regions of the HVMISFET and the LVMISFET being constituted as phosphorus impurity regions.

27. A semiconductor integrated circuit according to claim 26, wherein the minimum gate length in the channel length direction of the LVMISFET is in the range of 1.5 - 2.5 μm.

28. A semiconductor integrated circuit according to claim 26, wherein the HVMISFET comprises:

a source region and drain region of a second conductivity type formed apart from each other on a

surface of a semiconductor region of a first conductivity type,

a channel-forming region which is the surface of the semiconductor region between the source region and the drain region,

a gate formed on the channel-forming region via the gate insulating film,

the drain region being constituted of a low-concentration drain region and a high-concentration drain region in contact with each other,

the low-concentration drain region being disposed between the channel-forming region and the high-concentration drain region, and

a field insulating film with a thickness at least one order of ten greater than that of the gate insulating film formed by self-alignment above the low-concentration drain region.

29. A method of fabricating a semiconductor integrated circuit including an HVMISFET of a second conductivity type and an LVMISFET of the same conductivity type formed on a semiconductor region of first conductivity type, the method comprising the steps of:

forming an oxide mask film on the semiconductor region,

removing regions of the oxide-mask film to become an isolation region and a low-concentration drain region of the HVMISFET by etching using a photosensitive film,

implanting portions of the semiconductor region to become the low-concentration drain region with impurity ions of the second conductivity type using the oxide-mask film as a mask,

forming a field oxide film by selective oxidation of the surface of the semiconductor region using the oxide-mask film as a mask,

removing the oxide-mask film and forming a 100 - 200 Å insulating film on the semiconductor region to simultaneously form gate insulating films of the HVMISFET and the LVMISFET,

implanting the surface of the semiconductor region under the gate insulating films of the HVMISFET and the LVMISFET with impurity ions of the first conductivity type for defining a threshold voltage using the field insulating film as a mask,

patterning conductive films to become gates on the gate insulating films, and

forming a high-concentration drain region of the HVMISFET, a source region of the HVMISFET, a drain region of the LVMISFET and a source region of the LVMISFET by implanting ions of the second conductivity type using the gates and the field insulating film as a mask.

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